

In the claims

1. (Currently amended)

A method of manufacturing a plurality of micro
5 enclosures on a substrate wafer, comprising steps of:

(1) bonding a cap wafer to said substrate wafer with
an adhesive layer;

(2) patterning and etching said cap wafer and said
adhesive layer to form islands of layers of said cap wafer
10 and said adhesive layer on said substrate wafer; and

(3) depositing and patterning at least one metal
~~and/or insulator~~ layer on said islands to form a sidewall
around each of said islands.

15 2. (Previously presented)

The method of claim 1, further comprising the steps
of:

(1) patterning and etching etch access holes in said
cap wafer of said enclosures;

20 (2) removing said adhesive layer through said etch
access holes from said enclosures; and

(3) sealing said etch access holes with deposited
films.

25

4. (Original) The method of claim 1, wherein said etching
is accomplished with high-density plasma that contains
hydrogen or argon.

5. (Original) The method of claim 1, wherein said substrate wafer comprises one or more of following:

micro-electro-mechanical device,

5 polymeric sacrificial layer,

polymeric planarizing layer,

microelectronic circuit,

and electrical component,

prior to said bonding.

10

6. (Previously presented)

The method of claim 1, further comprising a step of depositing getters on said cap wafer prior to said step (1) of bonding a cap wafer to said substrate wafer with an adhesive layer and subsequent heat activation of said
15 getters.

7. (Previously presented)

The method of claim 2, wherein said deposited films
20 comprises gas gettering materials.

8. (Currently amended)

The method of claim 7, wherein said gettering materials comprise ~~one or more of the following:~~

25

TiN_xO_y and/or

~~TiZrx~~

TiNx

5

11. (Withdrawn)

The method of claim 2, wherein in said sealing is done
10 under controlled gas pressure environment comprising high
vacuum or inert gas.

12. (Withdrawn)

The method of claim 2, wherein said enclosures form
15 pressure transducers.

13. (Currently amended)

The method of claim 12, wherein said enclosures form
vacuum or hermetic packaging for micro-electro-mechanical
20 devices.

14. (Original)

The method of claim 2, wherein said removing said
adhesive layer is by etching with oxygenated plasma.

25

15. (Currently amended)

Said etching in claim 14 ~~further~~ removes ~~any~~ organic polymer coating or sacrificial layer ~~present~~ in said enclosures.

5 17. (Original)

The method of claim 1, wherein said depositing at least on metal layer is by physical vapor deposition, plating, electroplating, or chemical vapor deposition.

10 19. (Withdrawn)

The method of claim 1, further comprises planarizing said substrate wafer prior to said bonding, comprising steps of:

- coating said wafer with a thick epoxy layer;
- 15 curing said epoxy layer by heat or ultraviolet light; and
- thinning said epoxy layer to the desired thickness by lapping, grinding or polishing.

20 20. (Withdrawn)

The method of claim 19, wherein said thick epoxy layer fills holes, cavities, troughs, or underside space of suspended structures.

21. (Withdrawn)

- 25 The method of claim 20, further comprising the step of placing said wafer under a vacuum during or after said coating.

28. (Original)

The method of claim 1, wherein said adhesive layer is disposed by spinning and said spinning is at speed of between 1500 rpm to 7000 rpm for less than 2 seconds.

5

29. (Original)

The method of claim 1, wherein said adhesive layer comprises Abocast 50-24 epoxy resin from Abatron, Incorporated, Kenosha, WI 53144 USA.

10

30. (New) A plurality of sealed micro enclosures on a substrate wafer, each enclosure is enclosed by:

- (1) a top wafer bonded to said substrate wafer with an epoxy layer,
 - (2) a bottom formed from said substrate wafer, and
 - (3) a sidewall formed from at least one metal films,
- wherein said metal films are prepared by sputtering or evaporation deposition processes, said sidewall surround an island on said substrate wafer, and said island is formed from layers comprising said top wafer and said epoxy layer.

15

20